AMENDMENTS TO THE CLAIMS

1. **(Currently Amended)** A method comprising:

receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

generating a first data quantity value representing a quantity of data stored in the memory at a first point in time,

comparing the first data quantity value to a first predetermined value;

causing the transmitting device to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, in response to the comparing;

modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the second period of time is subsequent to the first period of time; and

wherein the second non-zero rate is greater than the first non-zero rate.

2. (Previously Presented) The method of claim 1 wherein the memory device comprises a FIFO buffer.

3. (Original) The method of claim 1 wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

4. (Previously Presented) The method of claim 1 further comprising:

generating a rate control signal; and

transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate;

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

5. (Cancelled)

6. (Previously Presented) The method of claim 4 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

7. (Previously Presented) The method of claim 4 further comprising:

generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

comparing the first data quantity value to the second data quantity value;

wherein the rate control signal is generated only if the first data quantity value is not equal to the second data quantity value.

8. (Previously Presented) The method of claim 1 wherein generating the first data quantity value comprises:

generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time;

generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time;

subtracting the total data output count from total data input count.

9. (Cancelled)

10. (**Currently Amended**) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate;

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time; ~~and~~

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing**; and**

a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value.

11. (Original) The apparatus of claim 10 wherein the memory device comprises a FIFO buffer.

12. (Original) The apparatus of claim 10 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

13. (Cancelled)

14. (Previously Presented) The apparatus of claim 10 further comprising:

a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined

values, wherein the first comparing circuit is one of the plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the first circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values.

15. (Previously Presented) The apparatus of claim 10 further comprising:

a third circuit for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

a second comparing circuit for comparing the first data quantity value to the second data quantity value;

wherein the first circuit generates the rate control signal only if the first data quantity value is not equal to the second data quantity value.

16. (Original) The apparatus of claim 15 wherein the first and second circuits are the same circuits.

17. – 23 (Cancelled)

24. (**Currently Amended**) An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate;

a second means for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time; ~~and~~

a third means for comparing the first data quantity value to a first predetermined value; **and**

a means for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the first means generates the rate control signal in response to the comparing.

25. (Original) The apparatus of claim 24 wherein the memory device comprises a FIFO buffer.

26. (Original) The apparatus of claim 24 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

27. (Previously Presented) The apparatus of claim 24 further comprising:

a fourth means for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

a fifth means for comparing the first data quantity value to the second data quantity value;

wherein the first means generates the rate control signal only if the first data quantity value is not equal to the second data quantity value.

28. (Cancelled)

29. (Cancelled)

30. (**Currently Amended**) A method comprising:

receiving data from a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

generating a rate control signal by

generating a first data quantity value representing a quantity of data stored in the memory at a first point in time, ~~and~~

comparing the first data quantity value to a first predetermined value, wherein

the rate control signal is generated in response to the comparing**;**

causing the transmitting device to transmit data at a second non-zero rate to the memory for storage therein during a second period of time, wherein

the causing comprises transmitting the rate control signal to the transmitting device; **and**

modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value;

wherein the second period of time is subsequent to the first period of time; and

wherein the second non-zero rate is less than the first non-zero rate.

31. **(Currently Amended)** An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate**,** wherein the second non-zero rate is less than the first non-zero rate;

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time; ~~and~~

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first circuit generates the rate control signal in response to the comparing**; and**

a circuit for modifying the first predetermined value in response at least in part to the comparing the first data quantity value to the first predetermined value.

32. (Previously Presented) The method of claim 30 further comprising:

transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate; and

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

33. (Cancelled)

34. (Previously Presented) The method of claim 32 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

35. (Previously Presented) The method of claim 1 wherein the causing comprises:

transmitting a rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate, wherein

the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

36. (Cancelled)

37. (Previously Presented) The method of claim 35 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

38. (Previously Presented) The method of claim 1 further comprising

the transmitting device transmitting data at a third non-zero rate to the memory for storage therein during a third period of time;

wherein the third period of time is subsequent to the second period of time, and wherein the third non-zero rate is greater than the second non-zero rate.

39. (Previously Presented) The method of claim 44, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

40. (Previously Presented) The apparatus of claim 45, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

41. (Previously Presented) The apparatus of claim 46, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

42. (Previously Presented) The apparatus of claim 47, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

43. (Previously Presented) The apparatus of claim 48, wherein the first predetermined value is modified to avoid frequent transmission of rate control signals due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

44. **(Cancelled)**

45. **(Cancelled)**

46. **(Cancelled)**

47. **(Cancelled)**

48. **(Cancelled)**